

CLAIMS

We claim:

- 5 1. A method for programming non-volatile memory, comprising:
 categorizing a set of non-volatile storage elements into three or more groups
 based on behavior of said non-volatile storage elements; and
 programming said non-volatile storage elements using a different programming
 condition for each group.
- 10 2. A method according to claim 1, wherein:
 said step of programming includes applying different bit line voltages for
 different groups.
- 15 3. A method according to claim 1, wherein:
 said step of programming includes applying a program signal to said non-volatile
 storage elements via a common word line and applying different bit line voltages for
 different groups.
- 20 4. A method according to claim 1, wherein:
 said step of categorizing includes determining programming speed information of
 said non-volatile storage elements relative to each other, each group including non-
 volatile storage elements with similar programming speed information.
- 25 5. A method according to claim 1, wherein:
 said step of categorizing includes determining programmability of said non-
 volatile storage elements relative to each other, each group including non-volatile storage

elements with similar programmability.

6. A method according to claim 1, wherein:

5 said step of categorizing includes applying one or more non-zero source voltages to said set of non-volatile storage elements and, while applying said one or more non-zero source voltages, characterizing threshold voltages of said set of non-volatile storage elements by applying one or more positive voltages to control gates for said non-volatile storage elements and determining whether said non-volatile storage elements turn-on in order to determine whether said non-volatile storage elements have a threshold voltage
10 greater than a negative voltage compare point.

7. A method according to claim 1, wherein:

said step of categorizing includes charging bit lines for said set of non-volatile storage elements, applying a control gate signal and allowing said bit lines to discharge;
15 and

said step of programming said non-volatile storage elements using a different programming condition for each group includes adjusting a subset of bit line voltages based on how said bit lines discharged.

20 8. A method according to claim 1, further comprising:

applying initial programming to said non-volatile storage elements prior to said step of programming said non-volatile storage elements using a different programming condition, said step of categorizing is based on said step of applying initial programming.

25 9. A method according to claim 8, wherein:

said initial programming and said step of programming said non-volatile storage elements using a different programming condition are performed using a common

program signal.

10. A method according to claim 9, wherein:
said common program signal is applied via a common word line; and
5 said step of adjusting includes determining which of said non-volatile storage elements are slow to program, determining which of said non-volatile storage elements are fast to program and raising a voltage on bit lines for said non-volatile storage elements that are determined to be fast to program.
- 10 11. A method according to claim 8, wherein:
said step of applying initial programming is performed until at least one non-volatile storage element reaches a target threshold value; and
said step of categorizing is performed for non-volatile storage elements that did not yet reach said target threshold value.
- 15 12. A method according to claim 1, wherein:
said non-volatile storage elements are multi-state storage elements.
13. A method according to claim 1, wherein:
20 said non-volatile storage elements are multi-state NAND flash memory elements.
14. A system for programming non-volatile memory, comprising:
a set of non-volatile storage elements;
a set of control lines in communication with said set of non-volatile storage
25 elements; and
a controlling circuit in communication with said control lines, said controlling circuit causes a categorizing of said set of non-volatile storage elements into three or

more groups based on behavior of said non-volatile storage elements and causes programming of said non-volatile storage elements using a different programming condition for each group.

- 5 15. A system according to claim 14, wherein:
 said control lines includes a set of bit lines and a common word line;
 said controlling circuit causes application of a program signal on said common
word line; and
 said different program condition for each group pertains to different bit line
10 voltages.

16. A system according to claim 14, wherein:
 said categorizing includes determining programming speed information of said
non-volatile storage elements relative to each other, each group including non-volatile
15 storage elements with similar speed information.

17. A system according to claim 14, wherein:
 said categorizing includes determining programming speed information of said
non-volatile storage elements relative to each other, each group including non-volatile
20 storage elements with similar speed information.

18. A system according to claim 14, wherein:
 said step of categorizing includes applying a non-zero source voltage to said set of
non-volatile storage elements and, while applying said non-zero source voltage,
25 characterizing threshold voltages of said set of non-volatile storage elements by applying
one or more positive voltages to control gates for said non-volatile storage elements and
determining whether said non-volatile storage elements turn-on in order to determine

whether said non-volatile storage elements have a threshold voltage greater than a compare point.

19. A system according to claim 14, wherein:
5 said categorizing includes charging bit lines for said set of non-volatile storage elements, applying a common control gate signal and allowing said bit lines to discharge; and
said programming of said non-volatile storage elements using a different programming condition for each group includes adjusting a subset of bit line voltages
10 based on how said bit lines discharged.

20. A system according to claim 14, wherein:
said controller circuit causes initial programming to said non-volatile storage elements prior to said programming said non-volatile storage elements using a different
15 programming condition, said categorizing is based on said initial programming.

21. A method according to claim 20, wherein:
said initial programming is performed until at least one non-volatile storage element reaches a target threshold value; and
20 said categorizing is performed for non-volatile storage elements that did not yet reach said target threshold value.

22. A system according to claim 20, wherein:
said initial programming is performed using a common word line signal.
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23. A system according to claim 14, wherein:
said non-volatile storage elements are multi-state storage elements.

24. A system according to claim 14, wherein:
said non-volatile storage elements are multi-state NAND flash memory elements.

5 25. A method for programming non-volatile memory, comprising:
applying initial programming to non-volatile storage elements until at least one
non-volatile storage element reaches a target threshold value; and
adjusting programming of at least a subset of non-volatile storage elements that
have not reached said target threshold value based on behavior of said non-volatile
10 storage elements that have not reached said target threshold value.

26. A method according to claim 25, further comprising:
characterizing said non-volatile storage elements that have not reached said target
threshold value based on programmability, said step of adjusting is based on said step of
15 characterizing.

27. A method according to claim 26, wherein:
said step of characterizing includes comparing a predetermined threshold voltage
to threshold voltages for said non-volatile storage elements that have not reached said
20 target threshold value.

28. A method according to claim 27, wherein:
said step of adjusting includes raising bit line voltages for non-volatile storage
elements that have threshold voltages greater than said predetermined threshold voltage.
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29. A method according to claim 25, further comprising:
said step of applying initial programming to non-volatile storage elements

includes applying a common program voltage signal to said non-volatile storage elements, said common program voltage signal increases at a first rate; and

said step of adjusting includes increasing said common program voltage signal above said first rate.

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30. A method according to claim 25, further comprising:

said step of applying initial programming to non-volatile storage elements and said step of adjusting include applying a common program voltage signal to said non-volatile storage elements.

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31. A method according to claim 25, further comprising:

said step of applying initial programming to non-volatile storage elements and said step of adjusting include applying a common program voltage signal to control gates of said non-volatile storage elements.

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32. A method according to claim 25, wherein:

said step of adjusting includes applying a non-zero source voltage to at least a subset of said non-volatile storage elements and comparing threshold voltages of said subset of non-volatile storage elements to a predetermined positive control gate value while applying said non-zero source voltage in order to determine programmability of said subset of non-volatile storage elements.

33. A method according to claim 25, wherein:
said step of adjusting includes charging bit lines for at least a subset of said non-volatile storage elements, applying a control gate signal to said subset of said non-volatile storage elements and allowing said bit lines to discharge; and
said step of adjusting further includes adjusting a subset of said bit line voltages

for programming based on how said bit lines discharged.

34. A method according to claim 25, wherein:
said non-volatile storage elements are multi-state storage elements.

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35. A method according to claim 25, wherein:
said non-volatile storage elements are multi-state NAND flash memory elements.

36. A system for programming non-volatile memory, comprising:
10 a set of non-volatile storage elements;
control lines in communication with said set of non-volatile storage elements; and
a controlling circuit in communication with said control lines, said controlling
circuit causes initial programming of said non-volatile storage elements until at least one
non-volatile storage element reaches a target threshold value, said controlling circuit
15 causes adjustment of programming of at least a subset of non-volatile storage elements
that have not reached said target threshold value based on behavior of said non-volatile
storage elements that have not reached said target threshold value.

37. A system according to claim 36, wherein:
20 said controlling circuit causes characterization of non-volatile storage elements
that have not reached said target threshold value based on programmability, said
adjustment of programming is based on said characterization.

38. A system according to claim 37, wherein:
25 said characterization includes comparing a predetermined threshold voltage to
threshold voltages for said non-volatile storage elements that have not reached said target
threshold, said predetermined threshold voltage is lower than said target threshold value.

39. A system according to claim 38, wherein:

said adjustment of programming includes raising bit line voltages for non-volatile storage elements that have threshold voltages greater than said predetermined threshold voltage.

40. A system according to claim 36, wherein:

said initial programming includes applying a common program voltage signal to said non-volatile storage elements, said common program voltage signal increases at a first rate; and

said adjustment of programming includes increasing said common program voltage signal above said first rate.

41. A system according to claim 36, wherein:

said initial programming includes applying a common program voltage signal to said non-volatile storage elements.

42. A system according to claim 36, wherein:

said adjustment of programming includes applying a non-zero source voltage to at least a subset of said non-volatile storage elements and comparing threshold voltages of said subset of non-volatile storage elements to a predetermined positive control gate value while applying said non-zero source voltage in order to determine programmability of said subset of non-volatile storage elements.

43. A system according to claim 36, wherein:

said adjustment of programming includes charging bit lines for at least a subset of said non-volatile storage elements, applying a control gate signal to said subset of said

non-volatile storage elements and allowing said bit lines to discharge; and
said adjustment of programming further includes adjusting a subset of said bit line
voltages for prgraming based on how said bit lines discharged.

5 44. A system according to claim 36, wherein:
 said non-volatile storage elements are multi-state storage elements.

 45. A system according to claim 36, wherein:
 said non-volatile storage elements are multi-state NAND flash memory elements.

10 46. A method for programming non-volatile memory, comprising:
 applying an initial program signal to a set of non-volatile storage elements;
 applying one or more non-zero source voltages to said set of non-volatile storage
 elements after commencing said initial program signal;
15 while applying said one or more non-zero source voltages, characterizing
 threshold voltages of said set of non-volatile storage elements by applying one or more
 positive voltages to control gates for said non-volatile storage elements and determining
 whether said non-volatile storage elements turn-on in order to determine whether said
 non-volatile storage elements have a threshold voltage greater than a compare point; and
20 adjusting a programming parameter of at least a subset of said non-volatile
 storage elements based on said step of characterizing.

 47. A method according claim 46, wherein:
 said compare point is a negative voltage.

25 48. A method according to claim 46, wherein:
 said initial program signal is applied via a common word line; and

said adjusting said programming parameter includes raising a voltage on one or more bit lines for said non-volatile storage elements.

49. A system for programming non-volatile memory, comprising:
- 5 a set of non-volatile storage elements;
control lines in communication with said set of non-volatile storage elements; and
a controlling circuit in communication with said control lines, said controlling circuit causes:
- 10 application of an initial program signal to said set of non-volatile storage elements,
- while applying one or more non-zero source voltages, characterization of threshold voltages of said set of non-volatile storage elements by applying a voltage to control gates for said non-volatile storage elements and determining whether said non-volatile storage elements turn-on in order to determine whether said non-volatile storage
- 15 elements have a threshold voltage greater than a compare point; and
adjustment of control line voltages of at least a subset of said non-volatile storage elements based on said step of characterizing.

50. A system according to claim 49, wherein:
- 20 said control lines includes a set of bit lines and a common word line;
said initial program signal is applied via said common word line; and
said adjustment of said control line voltages includes raising one or more bit line voltages.

- 25 51. A method for programming non-volatile memory, comprising:
applying an initial program signal to a non-volatile storage element;
applying a verify signal to a control gate for said of non-volatile storage element

after commencing said applying of said initial program signal;

charging a bit line for said of non-volatile storage element after commencing said
applying of said initial program signal;

allowing said bit line to discharge; and

5 adjusting a programming parameter of said non-volatile storage elements based
on said bit line discharging.

52. A method according to claim 51, wherein:

said initial program signal is applied via a common word line; and

10 said adjusting of said programming parameter includes raising a bit line voltage
for said non-volatile storage element for subsequent programming.

53. A method according to claim 51, wherein:

said non-volatile storage element is a flash memory device.

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54. A system for programming non-volatile memory, comprising:

a set of non-volatile storage elements;

a word line in communication with said set of non-volatile storage elements;

a set of bit lines in communication with said set of non-volatile storage elements;

20 and

a controlling circuit in communication with said word line, said control lines, and
said non-volatile storage elements, said controlling circuit causes:

application of an initial program signal to said non-volatile storage
elements,

25 application of a verify signal at a word line for said of non-volatile storage
elements after commencing said initial program signal,

charging of bit lines for said of non-volatile storage elements after

commencing said initial program signal,

allowing of said bit lines to discharge,

adjustment of a programming parameter of at least a subset of said non-volatile storage elements based on said bit line discharging, and

5 completion of programming of said non-volatile storage elements using said adjusted programming parameter.

55. A system according to claim 54, wherein:

said initial program signal is applied via said word line, said word line is common

10 to all said non-volatile storage elements; and

said adjustment of said programming parameter includes raising one or more of said bit lines.

56. A system according to claim 54, wherein:

15 said program parameter is adjusted differently for different non-volatile storage elements.

57. A system according to claim 54, wherein:

said non-volatile storage elements are flash memory devices.

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